Vihaan Patel

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EDUCATION

BSE Computer Systems Engineering (Honors) **May 2026**
Arizona State University, Tempe, AZ *GPA 3.9*

RESEARCH EXPERIENCE

Agentic AI for Coverage Closure in Hardware Verification *(Arizona State University)* ***August 2025 – Present***

- Built an agent orchestration system that autonomously generates stimulus (SystemVerilog) achieving 96-100% coverage across sub-system level hardware designs (up to 8,500 LOC), surfacing types of coverage holes that LLMs struggle with.
- Engineered domain-specialized tools, prompts, structured feedback loops, and a stateful workflow graph that shifted token allocation toward coverage-directed reasoning, yielding up to 4x token reduction over generic coding agents.

Deep Learning Undergraduate Research Fellow *(Arizona State University)* ***June 2024 – December 2024***

- Developed scalable Computer Vision pipelines using PyTorch on HPC clusters to benchmark ConvNext and Detectron2 for complex pattern recognition tasks including classification, localization, and segmentation.
- Optimized Mask R-CNN architectures via custom data augmentations and supervised fine-tuning, successfully increasing model precision for automated defect identification and anomaly detection applications.

RELEVANT PROJECTS

UVM Verification of FIFO, MIPS Pipeline, and Systolic Array ***Summer 2025***

- Developed UVM verification environments using object-oriented SystemVerilog to create reusable agents, sequences, and scoreboards for an asynchronous FIFO, a pipelined MIPS processor, and a systolic array accelerator.
- Authored verification plans, driving stimulus with constrained-random tests in VCS and closing functional/code coverage goals in Verdi to validate micro-architectural features like hazard forwarding and memory-mapped control.

Agentic Workspace for GPU optimization ***Summer 2025***

- Built GPU-acceleration infrastructure utilizing NVIDIA RAPIDS (cuDF, cuML, CuPy) to standardize ETL data analytics pipelines, automate performance profiling, and deliver 3x speed-up on large-scale data workloads.
- Deployed a production-grade AI inference service on HPC clusters, utilizing robust state management and vector search (ChromaDB) to support complex query workflows; NVIDIA AI Spark Challenge Awardee

FPGA Systolic Array and Multi-Cycle MIPS Extension ***Fall 2024***

- Built and debugged a 4x4 systolic-array matrix-multiplier with custom MAC units and BRAM integration; fixed RAM/PE bugs, completed datapaths, and validated the design using structured testbenches and timing-driven simulation.
- Extended a multi-cycle MIPS processor by adding a MULT16 instruction, updating ALU and memory initialization, and deploying it on an Artix-7 FPGA with slow-clock control, HALT/RESET support, and an LED-driven rotation program.

WORK EXPERIENCE

Lead Tutor, Academic Support Network *(Arizona State University)* ***January 2025 – Present***

- Spearheaded the curriculum design and delivery of high-impact review sessions for CS, Math, and Physics, standardizing tutoring methodologies to ensure consistency across a network of 20,000+ students.
- Partnered with university faculty to execute campus-wide technical workshops, successfully scaling academic support operations and bridging the communication gap between course requirements and student success.

SKILL SET

- **Programming:** Python, C++, Java, Bash/Shell, SQL
- **Hardware Design & Verification:** SystemVerilog, Vivado, VCS, Verdi, UVM, Constrained-Random Testing, FPGAs
- **GenAI Systems:** LangChain/LangGraph, HuggingFace, RAG, Vector Stores, MCP, Prompt Engineering
- **Infrastructure:** vLLM, CUDA, RAPDIS, TensorRT, HPC/SLURM, Linux, Docker, Kubernetes, AWS EC2, Git
- **Machine Learning:** PyTorch, TensorFlow/Keras, CNNs, Supervised Fine-tuning and Reinforcement Learning